UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,948	01/23/2004	Chantal J. Arena	ASMEX.425A	5065

20995 7590 04/27/2005

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/763,948	ARENA ET AL.
	Examiner	Art Unit
	PHUC T. DANG	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15 and 30-41* is/are allowed.

6)☒ Claim(s) *16,17,21,22 and 27* is/are rejected.

7)☒ Claim(s) *18-20,23-26,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *050504*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application claims benefit of 60/442,694 filed on January 24, 2003.

Oath/Declaration

2. The oath/declaration filed on January 23, 2004 is acceptable.

Information Disclosure Statement

3. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on May 5, 2004.

Specification

4. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishiguchi et al., herinafter "Shishiguchi" (U.S. Patent No. 6,190,976) in view of Asakawa (U.S. Publication No. US 2001/0046766 A1).

Regarding claim 16, Shishiguchi discloses a method comprising:

providing a semiconductor substrate (1, Fig. 1A) having a gate (4, Fig. 2A) and exposed active areas (6a, 6b, Fig. 2A);

depositing polycrystalline silicon (8c, Fig. 2A) on the gate (4, Fig. 2A) and epitaxial silicon on the active areas (6a, 6b, Fig. 2A) in a first process step.

Shishiguchi discloses all the features of the claimed invention as discussed above, but does not disclose a step of etching polycrystalline silicon from the gate in a second process step.

Asakawa, however, discloses a step of etching polycrystalline silicon (17, Fig. 1(b)-1(c)) from the gate (19, Fig. 1(b)-1(c) in a second process step [[0058]-[0064] page 4-5].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Shishiguchi discussed above as taught by Asakawa for a purpose of eliminating excessive polycrystalline silicon deposition on the gate structure.

Shishiguchi discloses all the features of the claimed invention as discussed above, but does not disclose a step of repeating the firs and second process steps a plurality of times.

Repeating the firs and second process steps a plurality of times is considered to be obvious in variation design, since any step can repeat as many times as it can during in the process. Thus, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching Shishiguchi discussed above as taught by the above teaching for a purpose of improving the process.

Regarding claim 21, Shishiguchi discloses during the first process step, polycrystalline silicon deposition and epitaxial silicon deposition occur simultaneously [col. 6, lines 32-41].

Regarding claim 22, Asakawa discloses the second process step comprises simultaneously etching epitaxial silicon from the active area [Fig. 2© and [0065] page 5].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching Shishiguchi discussed above as taught by Asakawa for a purpose of improving the process.

6. Claims 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishiguchi et al., herinafter "Shishiguchi" (U.S. Patent No. 6,190,976) in view of admitted Applicant's Prior art (AAPA).

Regarding claim 17, Shishiguchi discloses all the features of the claimed invention as discussed above, but does not disclose a step of the semiconductor substrate further comprises an oxide region, and wherein no silicon is deposited on the oxide region during the first process step.

(AAPA), however, discloses a step of the semiconductor substrate further comprises an oxide region, and wherein no silicon is deposited on the oxide region during the first process step [[0005] page 2 on specification].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching Shishiguchi discussed above as taught by AAPA for a purpose of eliminating excessive polycrystalline silicon deposition on the gate structure.

7. SHishiguchi discloses the claimed invention except for the process parameters as claimed in claim 27. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to prevent excessive polycrystalline silicon deposition on the gate structure, since it is well settle that when the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Allowable Subject Matter

8. Claims 1-15 and 30-41 would be allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claims 1-15 and 30-41 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention having a layer of a step of performing a flash etch back process in which the polycrystalline layer is etched from the gate at a first etching rate and the epitaxial layer is etched from the active areas at a second etching rate, wherein the first etching rate is faster than the second etching rate as disclosed in claim 1 and a step of controlling the epitaxial growth rate and the polycrystalline growth rate by periodically pausing the epitaxial growth and the polycrystalline growth to perform a flash etch back process, such that aûer the flash etch back process there is more epitaxial growth on the first growth surface than polycrystalline growth on the second growth surface as cited in claim 30 and a step of alternating a selective epitaxial growth process, during which epitaxial growth comprising polycrystalline growth and monocrystalline growth

occurs in the at least one non-oxide region and during which substantially no deposition occurs in the at least one oxide region, with a flash etch back process, during which at least a portion of the polycrystalline growth is etched from the at least one non-oxide region as cited in claim 36.

Claims 18-20, 23-26 and 28-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because these claims are depend the independent claim 18.

None of the Prior Art made of record discloses wherein during the second process step polycrystalline silicon is etched in two orthogonal dimensions as cited in claim 18 and wherein the polycrystalline silicon is etched from the gate faster than the epitaxial silicon is etched from the active areas during the second process step as cited in claim 23 and wherein silicon is not deposited onto the semiconductor substrate during the second process step as cited in claim 24 and wherein the first process step is conducted at a lower temperature than the second process step as cited in claim 25 and wherein the semiconductor substrate is exposed to hydrochloric acid during the second process step as cited in claim 28 and wherein the semiconductor substrate is held at a pressure substantially equal to atmospheric pressure during the second process step as cited in claim 29.

Claims 19-20 and 26 are directly or indirectly on claims 18 and 25, then they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

11. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818